

# HMF65N180E7

## N-Channel eMOS E7 Power MOSFET

650 V, 19 A, 180 mΩ

### Description

The 650V eMOS E7 is an advanced Power Master Semiconductor's Super Junction MOSFET family by utilizing charge balance technology for excellent low on-resistance and gate charge.

This technology combines the benefits of an excellent switching performance with ease of usage and robustness.

Consequently, the 650V eMOS E7 family is suitable for application requiring superior efficiency and extra safety margin for design with higher voltage.

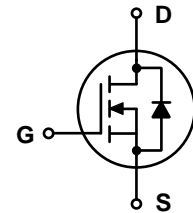
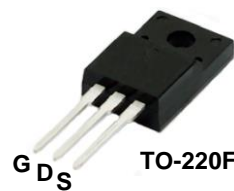
### Applications

- PFC, Hard & Soft Switching Topologies
- Industrial & Consumer Power Supplies

### Features

$BV_{DSS} @ T_{J,max}$	$I_D$	$R_{DS(on),max}$	$Q_{g,typ}$
700 V	19 A	180 mΩ	32.1 nC

- Reduced Switching & Conduction Losses
- Lower Switching Noise
- 100% Avalanche Tested
- Pb-free, Halogen Free, and RoHS Compliant



### Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ\text{C}$ )	19*
		Continuous ( $T_C = 100^\circ\text{C}$ )	12*
$I_{DM}$	Drain Current	Pulsed (Note1)	53*
$E_{AS}$	Single Pulsed Avalanche Energy	(Note2)	103
$I_{AS}$	Avalanche Current	(Note2)	4
$E_{AR}$	Repetitive Avalanche Energy	(Note1)	1.62
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt	(Note3)	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	36
		Derate Above $25^\circ\text{C}$	0.29
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds	260	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
HMF65N180E7	HMF65N180E7	TO-220F	Tube	50 units

Electrical Characteristics ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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## Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	700			
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		2		
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

## On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1.7\text{ mA}$	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}$		150	180	m $\Omega$

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 250\text{ kHz}$		1233		pF
$C_{oss}$	Output Capacitance			35		pF
$C_{o(tr)}$	Time Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		402		pF
$C_{o(er)}$	Energy Related Output Capacitance			54		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400\text{ V}, I_D = 8.5\text{ A},$ $V_{GS} = 10\text{ V}$		32.1		nC
$Q_{gs}$	Gate to Source Charge			6.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			16		nC
$R_G$	Gate Resistance	$f = 1\text{ MHz}$		6.9		$\Omega$

## Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 400\text{ V}, I_D = 8.5\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 10\ \Omega$ See Figure 13		15		ns
$t_r$	Turn-On Rise Time			11		ns
$t_{d(off)}$	Turn-Off Delay Time			71		ns
$t_f$	Turn-Off Fall Time			11		ns

## Source-Drain Diode Characteristics

$I_S$	Maximum Continuous Diode Forward Current			19		A
$I_{SM}$	Maximum Pulsed Diode Forward Current			57		A
$V_{SD}$	Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 8.5\text{ A}$			1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 8.5\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		284		ns
$Q_{rr}$	Reverse Recovery Charge			3.46		$\mu\text{C}$

※Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 4\text{ A}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 8.5\text{ A}, di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 400\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

Typical Performance Characteristics

Figure 1. On-Region Characteristics

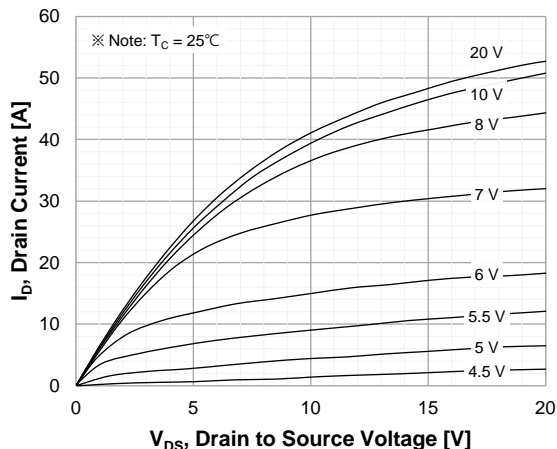


Figure 2. Transfer Characteristics

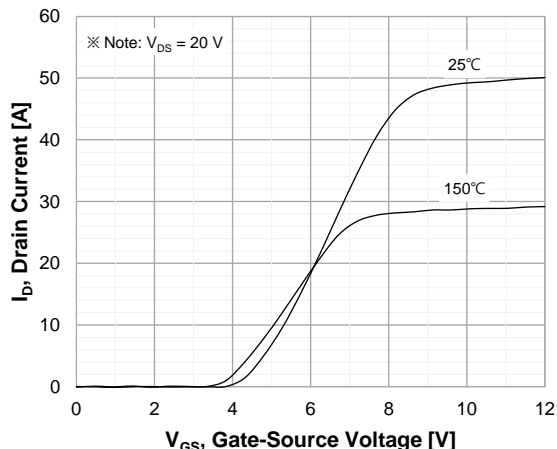


Figure 3. On-Resistance Characteristics vs. Drain Current and Gate Voltage

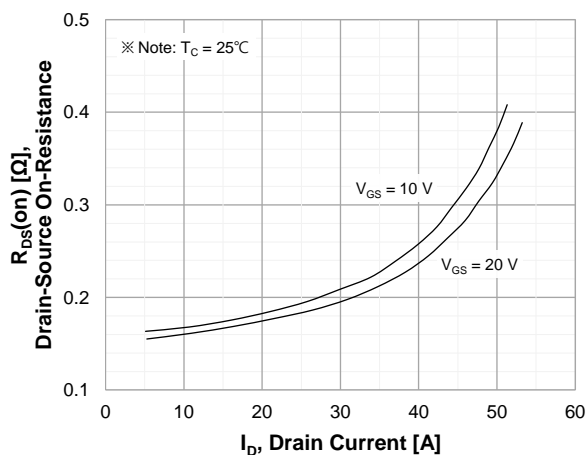


Figure 4. Diode Forward Voltage Characteristics vs. Source-Drain Current and Temperature

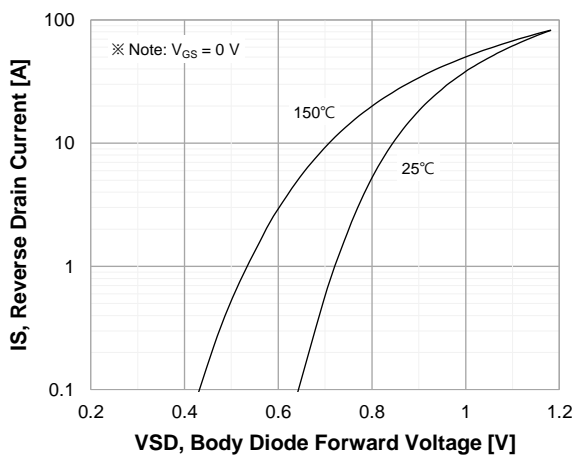


Figure 5. Capacitance Characteristics

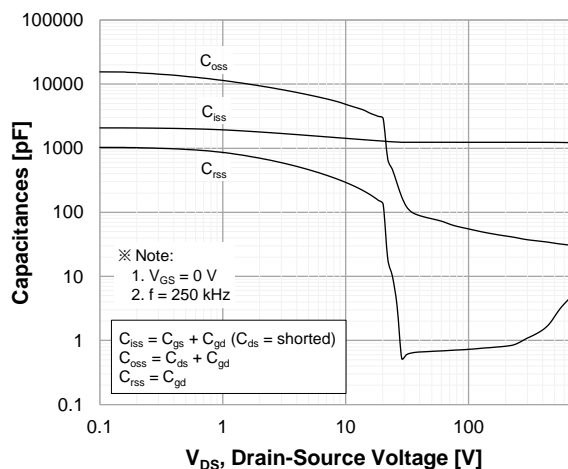
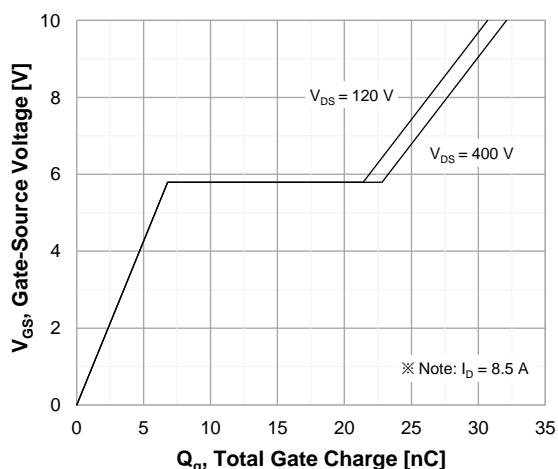


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Characteristics vs. Temperature

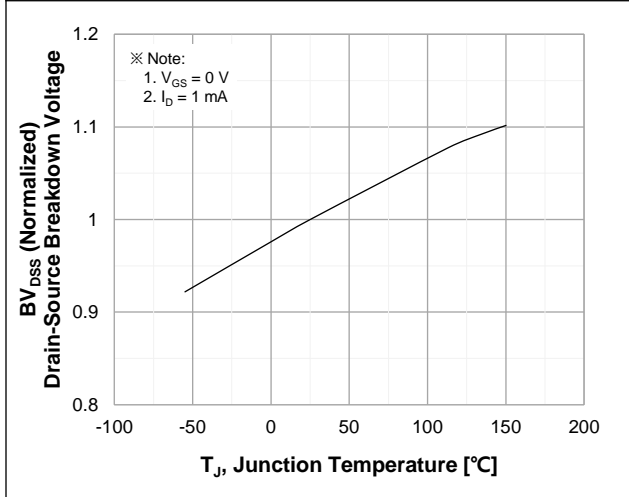


Figure 8. On-Resistance Characteristics vs. Temperature

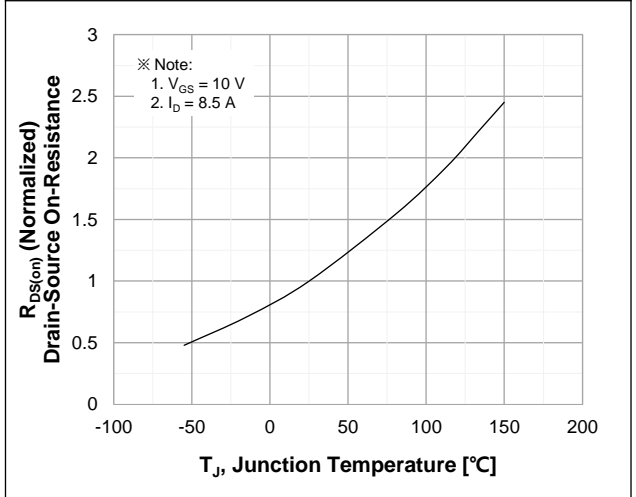


Figure 9. Maximum Safe Operating Area

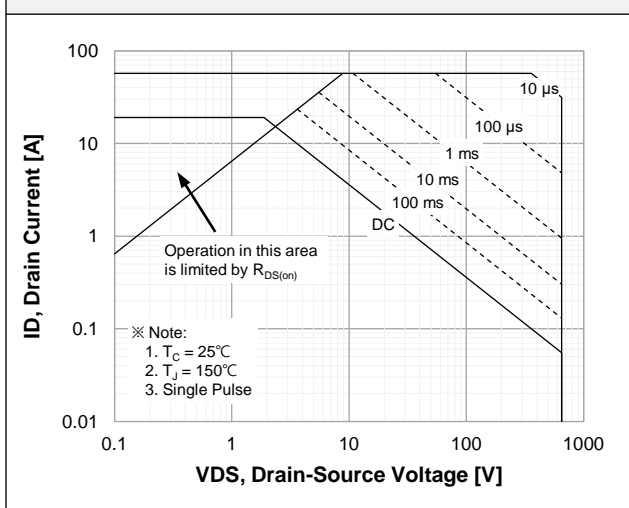


Figure 10. Maximum Drain Current vs. Case Temperature

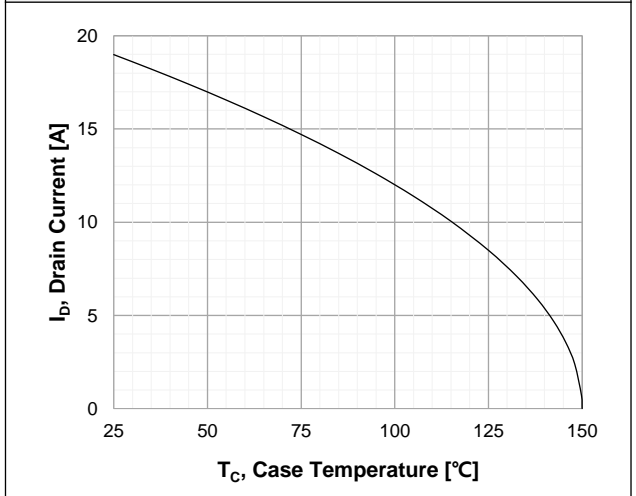


Figure 11. E\_oss vs. Drain to Source Voltage

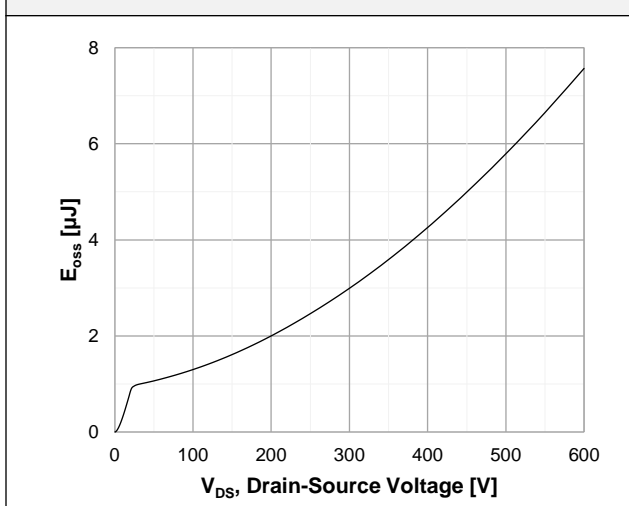
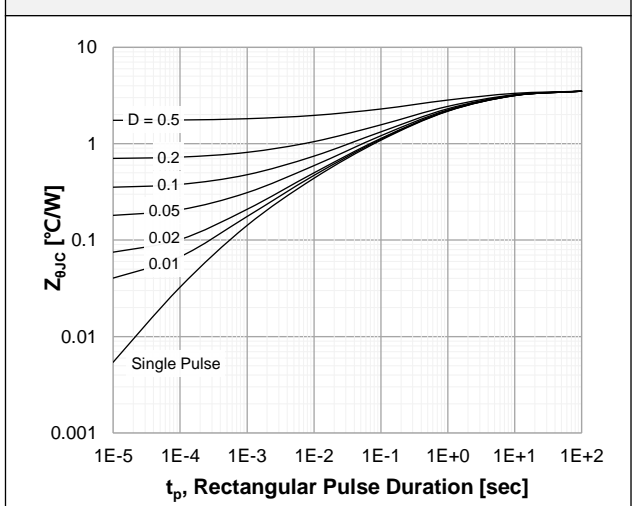


Figure 12. Transient Thermal Response Curve



Test Circuits

Figure 13. Inductive Load Switching Test Circuit and Waveforms

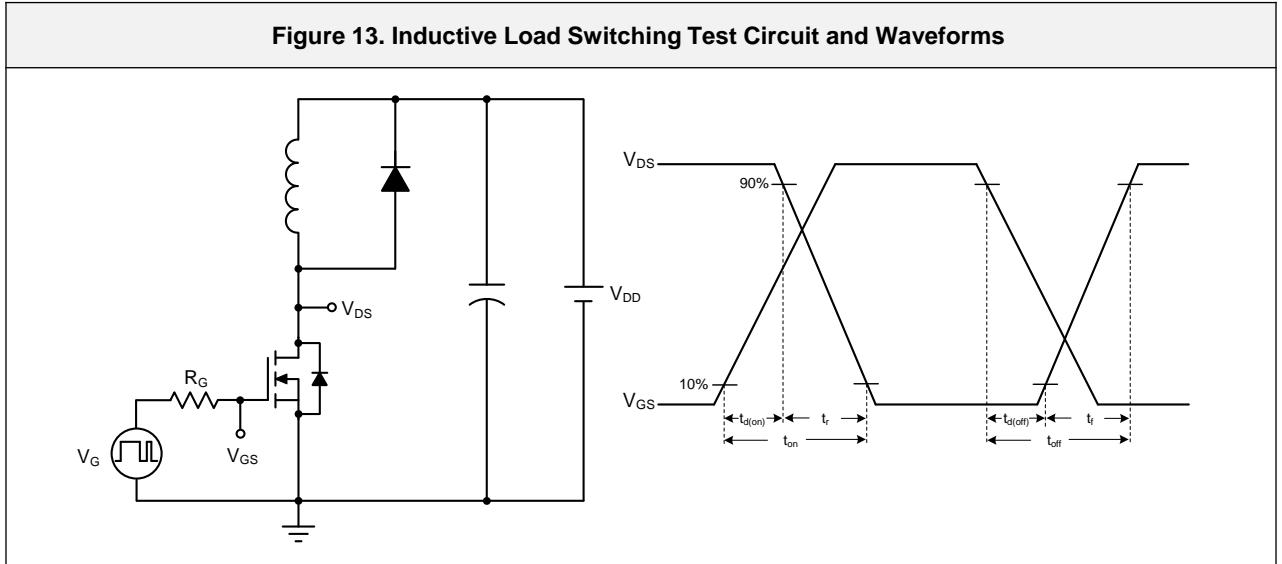


Figure 14. Unclamped Inductive Switching Test Circuit and Waveforms

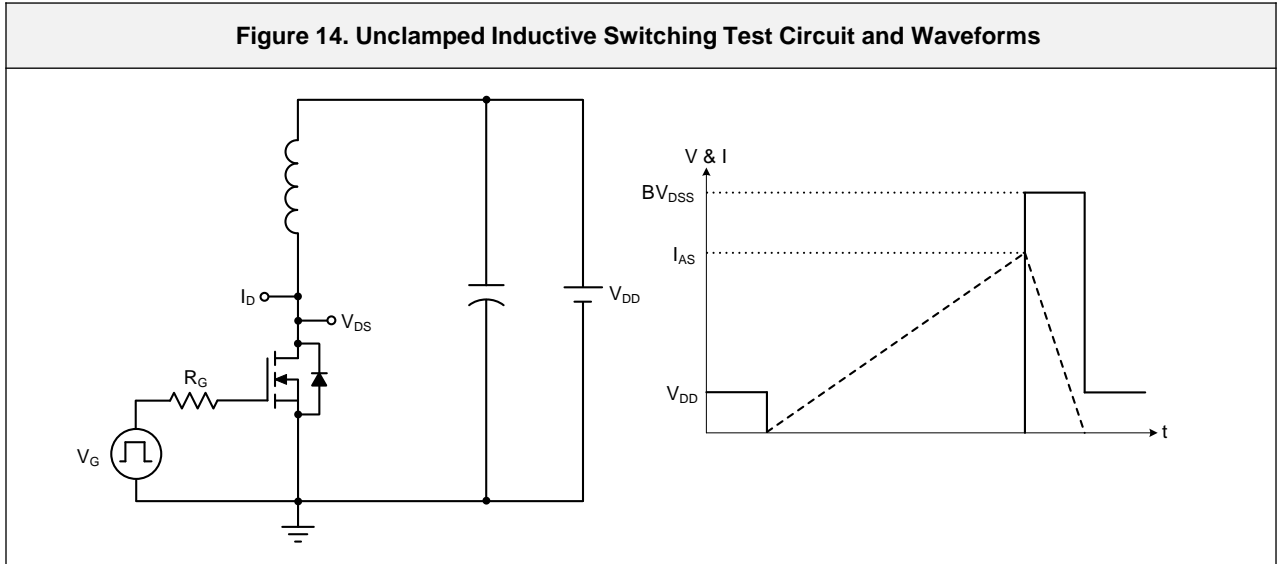
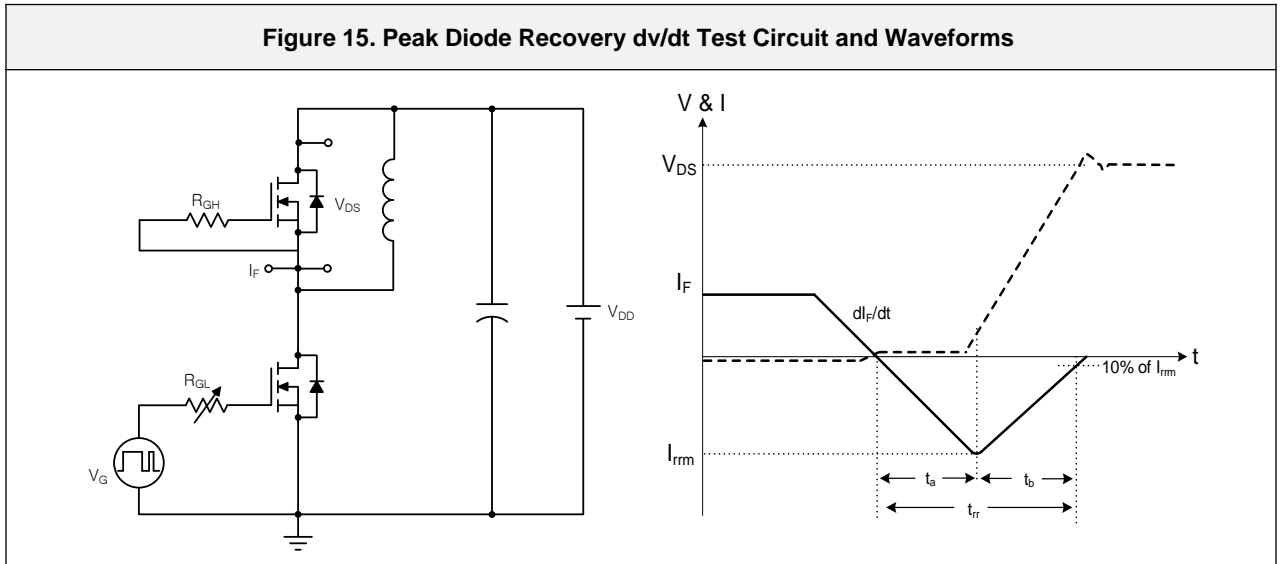
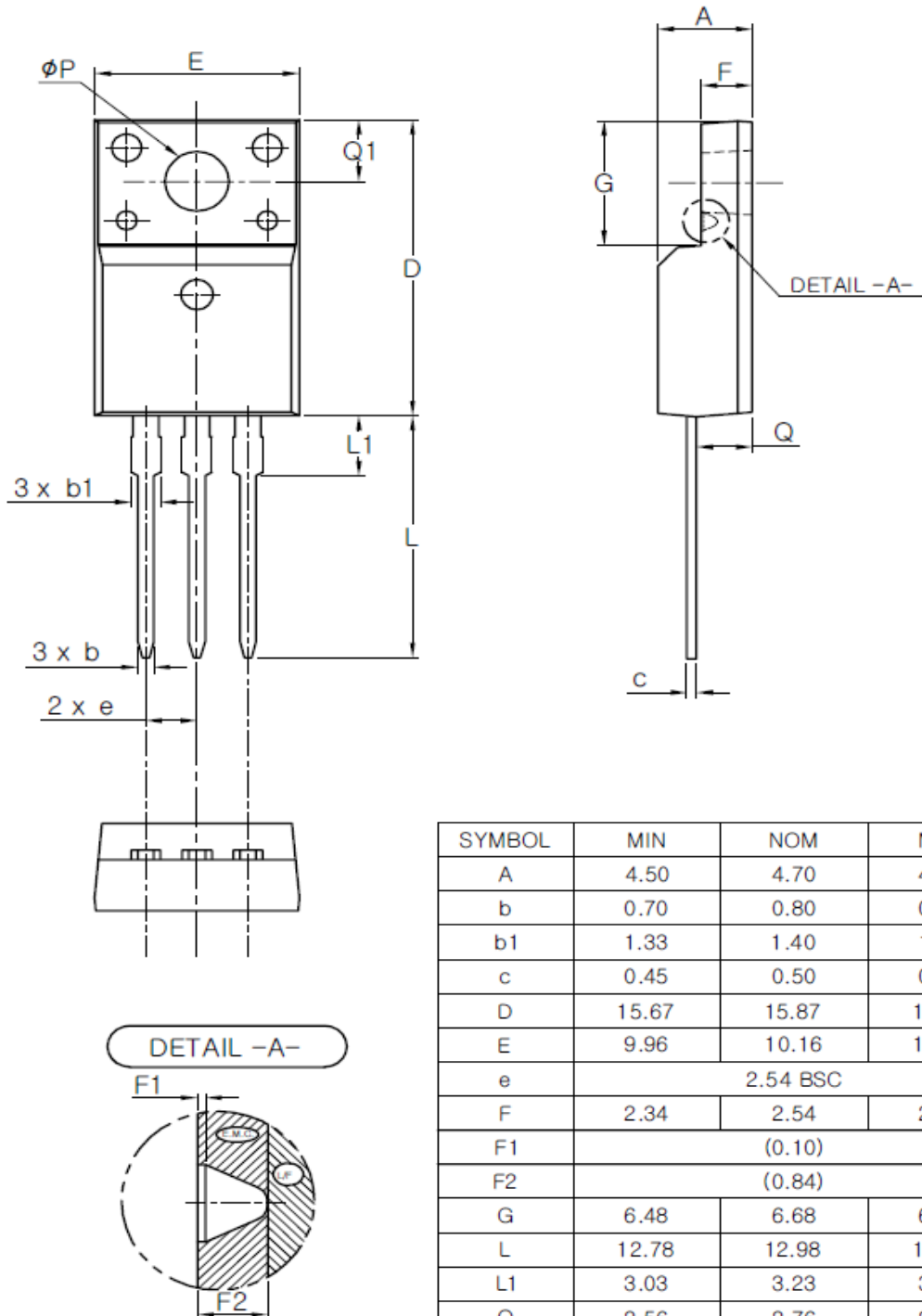


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit and Waveforms



Package Outlines

TO-220F



SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.90
b	0.70	0.80	0.90
b1	1.33	1.40	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
E	9.96	10.16	10.36
e	2.54 BSC		
F	2.34	2.54	2.74
F1	(0.10)		
F2	(0.84)		
G	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Q	2.56	2.76	2.96
Q1	3.10	3.30	3.50
$\phi P$	3.08	3.18	3.28

\* Dimensions in millimeters