

HCRZ120N40M2A

N-Channel eSiC Silicon Carbide Power MOSFET

1200 V, 57 A, 40 mΩ

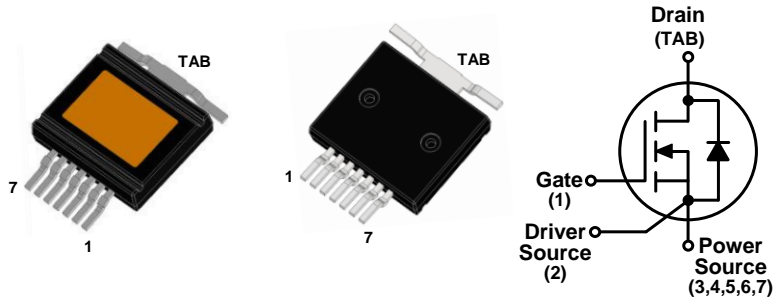
Features

- High switching speed with a low gate charge
- Isolated substrate / High dielectric strength
- Isolation rating of 3.6kVrms
- 100% Avalanche Tested
- Pb-free, Halogen Free, and RoHS Compliant
- AEC Q101 Qualified

$BV_{DSS, T_C=25^\circ C}$	$I_D, T_C=25^\circ C$	$R_{DS(on), typ}$	$Q_{g, typ}$
1200 V	57 A	40 mΩ	62 nC

Benefits

- Top-side-cooling package
- Longer clearance / creepage distance
- Kelvin source connection
- Higher frequency applicability
- Easy heatsink assembly with thermal grease



Applications

- Automotive applications (OBC, e-Comp, DC/DC)
- Solar inverter
- EV charging station
- UPS, Industrial power supply



Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	1200	V
V_{GS}	Gate to Source Voltage (DC)	-10 / +22	V
V_{GSop}	Recommended Operation Value	-5...-3 / +18	V
I_D	Drain Current	Continuous ($T_C = 25^\circ C$)	57
		Continuous ($T_C = 100^\circ C$)	40
I_{DM}	Drain Current	Pulsed (Note1)	142
P_D	Power Dissipation	($T_C = 25^\circ C$)	156
		Derate Above $25^\circ C$	1.9
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 175	$^\circ C$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds	260	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.96	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
HCRZ120N40M2A	HCRZ120N40M2A	TO-263-7L V2 (DBC)	Tape and Reel	700 units

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$		1	100	μA
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$		10		
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = +22\text{ V}, V_{DS} = 0\text{ V}$			+100	nA
		$V_{GS} = -10\text{ V}, V_{DS} = 0\text{ V}$			-100	

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 10\text{ mA}$ (tested after $V_{GS} = 22\text{ V}, 1\text{ ms pulse}$)	2.0	3.0	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 18\text{ V}, I_D = 28\text{ A}$		40.0	54.0	$\text{m}\Omega$
		$V_{GS} = 18\text{ V}, I_D = 28\text{ A}, T_J = 175^\circ\text{C}$		64.0		
		$V_{GS} = 15\text{ V}, I_D = 28\text{ A}$		55.5		
g_{fs}	Transconductance	$V_{DS} = 20\text{ V}, I_D = 28\text{ A}$		16.9		S

Dynamic Characteristics

C_{iss}	Input Capacitance			1668		pF
C_{oss}	Output Capacitance	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$		105		
C_{riss}	Reverse Capacitance			4		
E_{oss}	Stored Energy in Output Capacitance			42		μJ
$C_{o(er)}$	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to } 800\text{ V}, V_{GS} = 0\text{ V}$		132		pF
$C_{o(tr)}$	Time Related Output Capacitance			201		
$Q_{g(tot)}$	Total Gate Charge	$V_{DS} = 800\text{ V}, I_D = 28\text{ A},$ $V_{GS} = -3\text{ V} / 18\text{ V},$ Inductive load		62		nC
Q_{gs}	Gate to Source Charge			20		
Q_{gd}	Gate to Drain "Miller" Charge			14		
R_G	Internal Gate Resistance	$f = 1\text{ MHz}, V_{AC} = 30\text{ mV}$		3.0		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 800\text{ V}, I_D = 28\text{ A},$ $V_{GS} = -3\text{ V} / 18\text{ V}, R_G = 6.8\ \Omega,$ FWD : PCH120S20D1, Inductive load		19		ns
t_r	Turn-On Rise Time			15		
$t_{d(off)}$	Turn-Off Delay Time			35		
t_f	Turn-Off Fall Time			8		μJ
E_{on}	Turn-on Switching Energy			158		
E_{off}	Turn-off Switching Energy			100		
E_{tot}	Total Switching Energy			258		

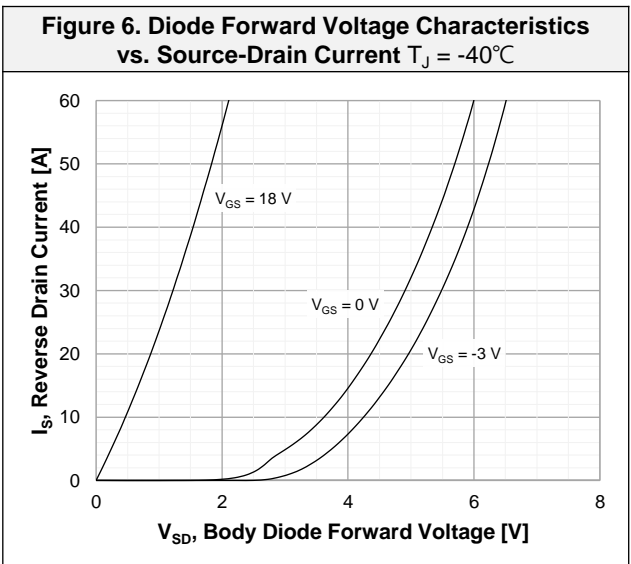
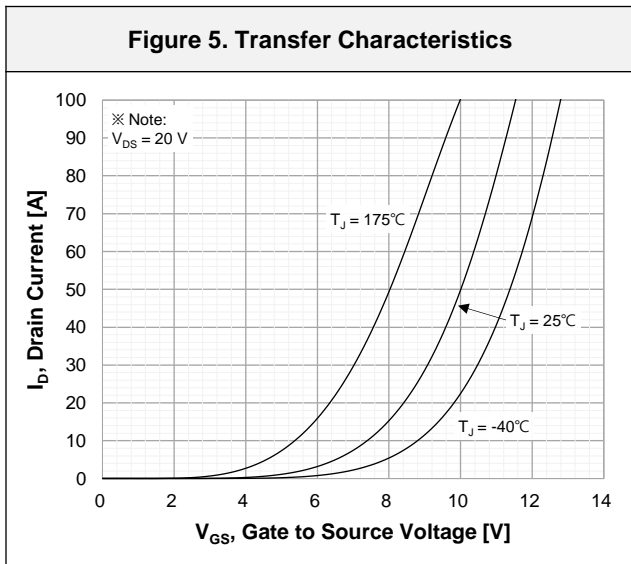
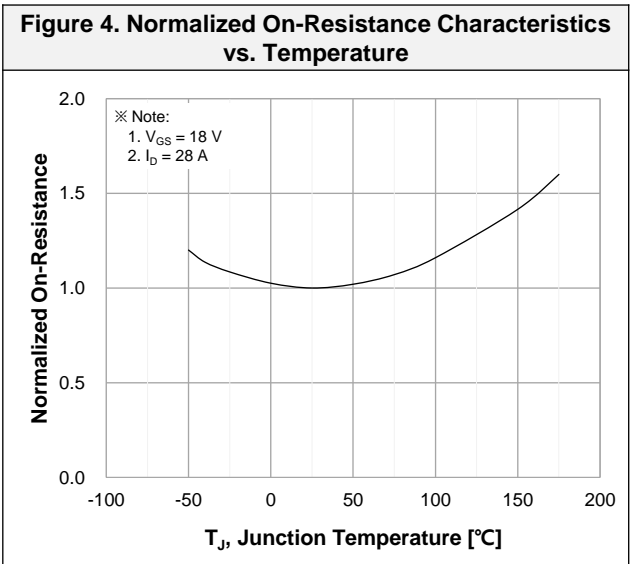
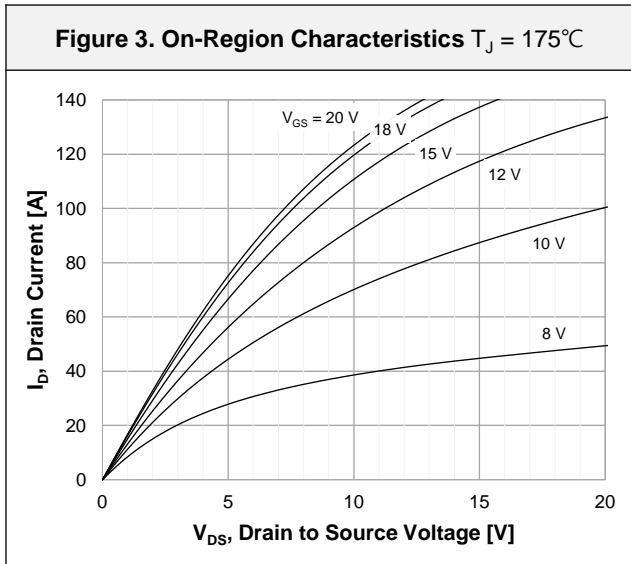
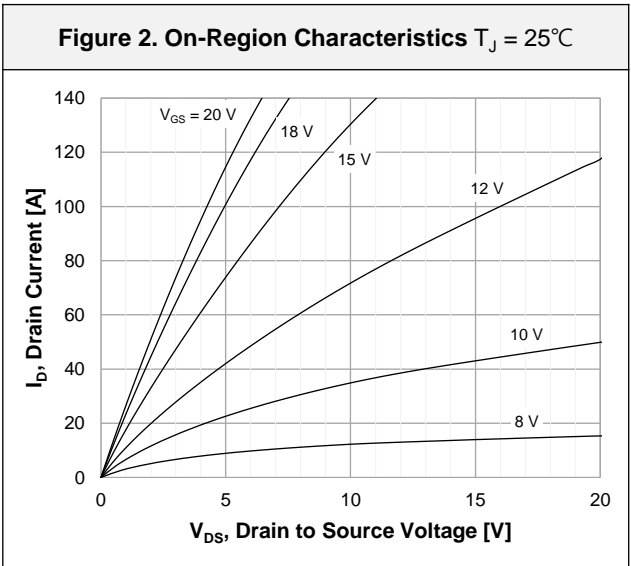
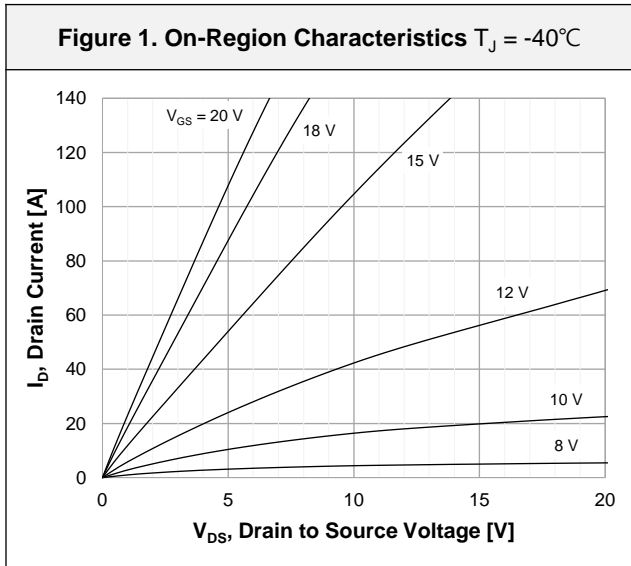
Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Source-Drain Diode Characteristics						
I_S	Continuous Diode Forward Current	$V_{GS} = -3\text{ V}$			57	A
I_{SM}	Pulsed Diode Forward Current	$V_{GS} = -3\text{ V}$ (Note1)			142	
V_{SD}	Diode Forward Voltage	$V_{GS} = -3\text{ V}, I_{SD} = 28\text{ A}$		4.3		V
t_{rr}	Reverse Recovery Time	$V_{DD} = 800\text{ V}, I_{SD} = 28\text{ A},$ $di_F/dt = 3000\text{ A}/\mu\text{s},$ Includes Q_{oss}		15		ns
Q_{rr}	Reverse Recovery Charge			219		nC
I_{rrm}	Peak Reverse Recovery Current			24		A

※Note 1 : Limited by maximum junction temperature.

※Note 2 : DBC discoloration and Picker Circle Printing allowed.

Typical Performance Characteristics



Typical Performance Characteristics

Figure 7. Diode Forward Voltage Characteristics vs. Source-Drain Current $T_J = 25^\circ\text{C}$

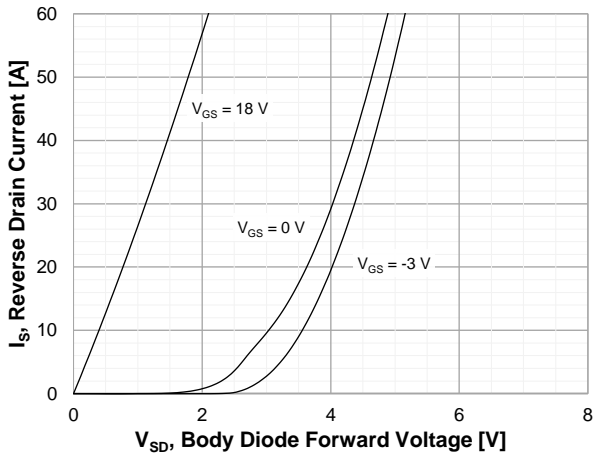


Figure 8. Diode Forward Voltage Characteristics vs. Source-Drain Current $T_J = 175^\circ\text{C}$

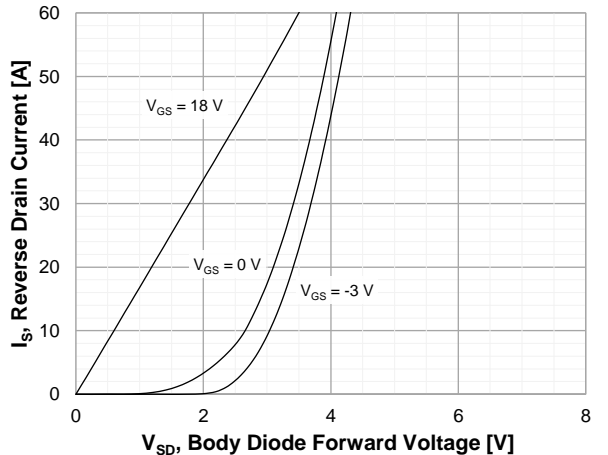


Figure 9. Threshold Voltage vs. Temperature

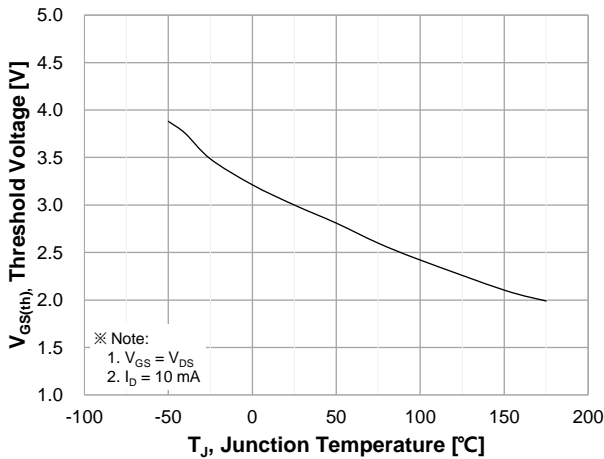


Figure 10. Gate Charge Characteristics

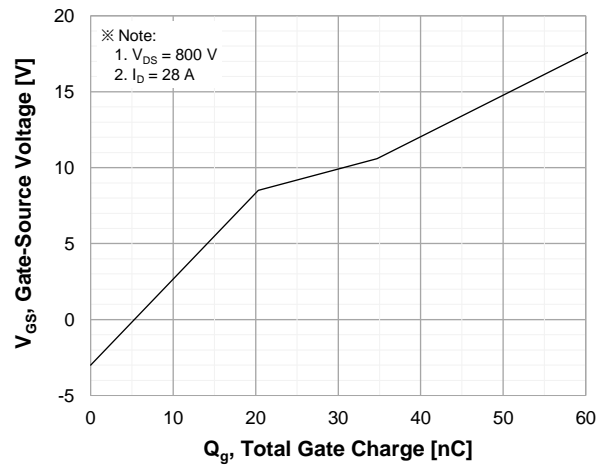


Figure 11. Stored Energy in Output Capacitance

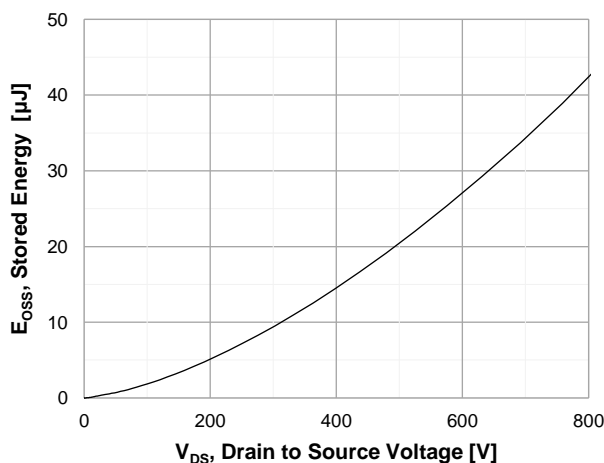
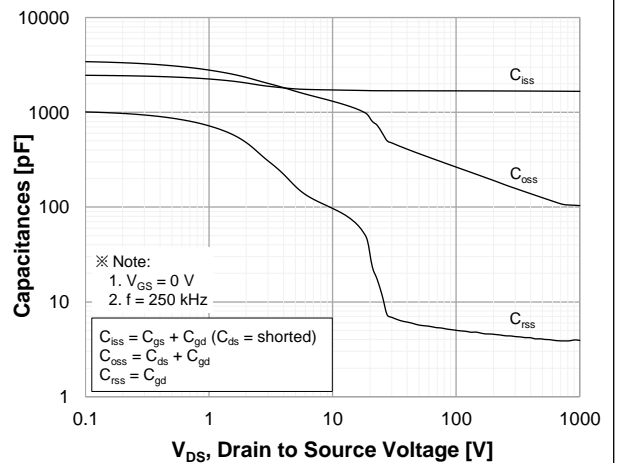


Figure 12. Capacitance Characteristics



Typical Performance Characteristics

Figure 13. Continuous Drain Current Derating vs. Case Temperature

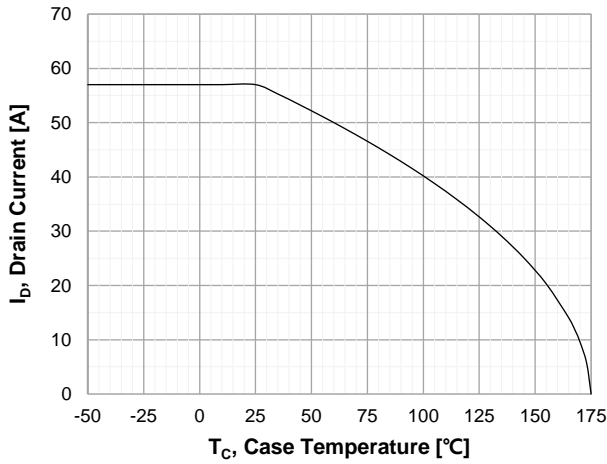


Figure 14. Maximum Power Dissipation Derating vs. Case Temperature

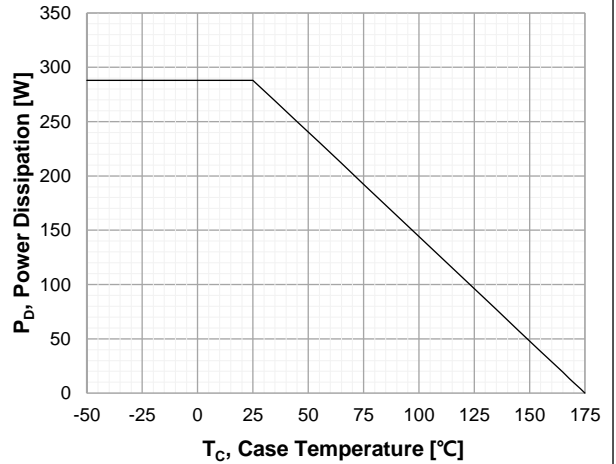


Figure 15. Typ. Switching Losses vs. Drain Current

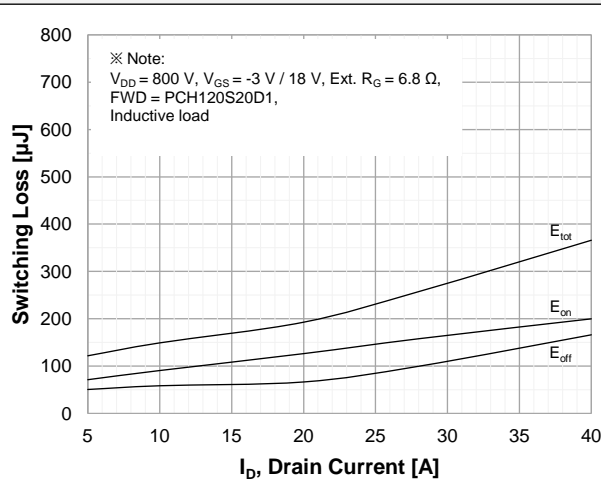


Figure 16. Typ. Switching Losses vs. Gate Resistance

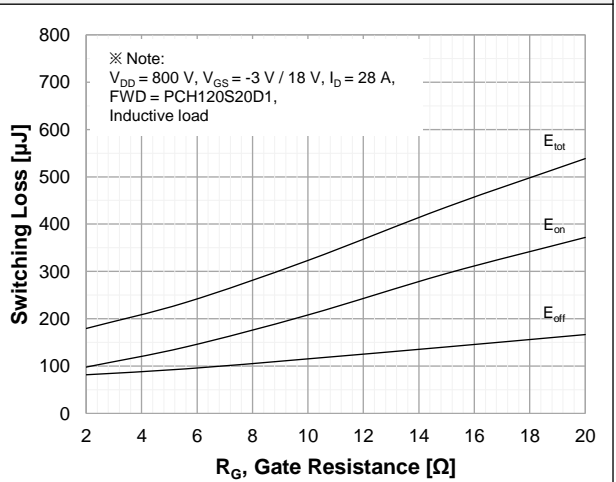


Figure 17. Typ. Switching Losses vs. Drain Current

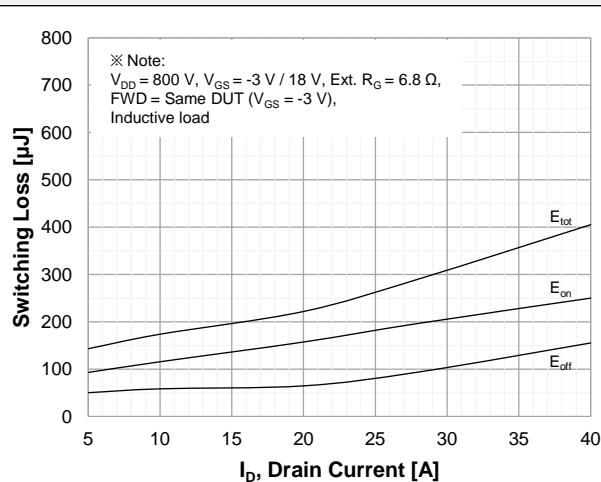
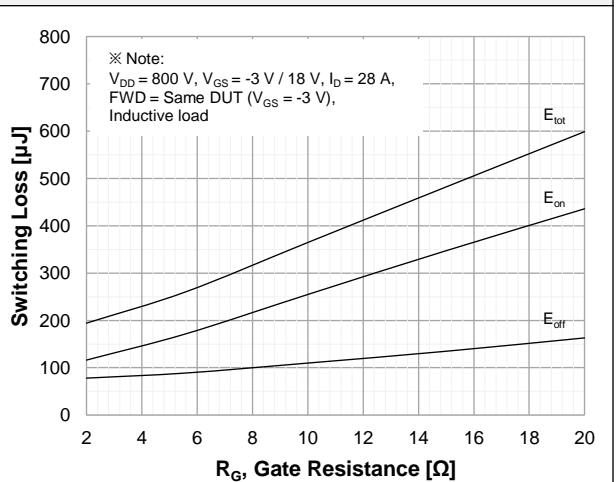


Figure 18. Typ. Switching Losses vs. Gate Resistance



Typical Performance Characteristics

Figure 19. Maximum Safe Operating Area

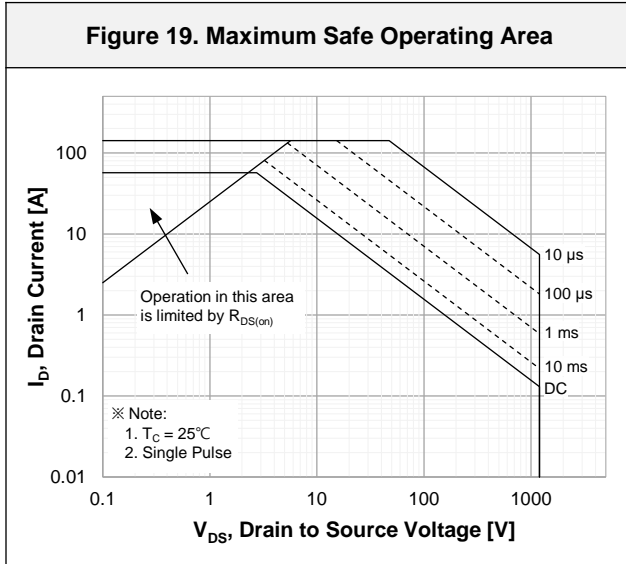


Figure 20. Transient Thermal Response Curve

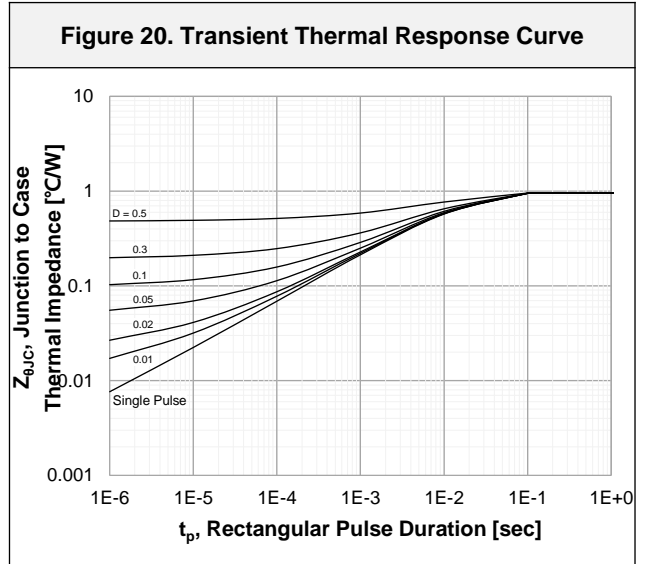


Figure 21. Inductive Load Switching Test Circuit and Waveforms

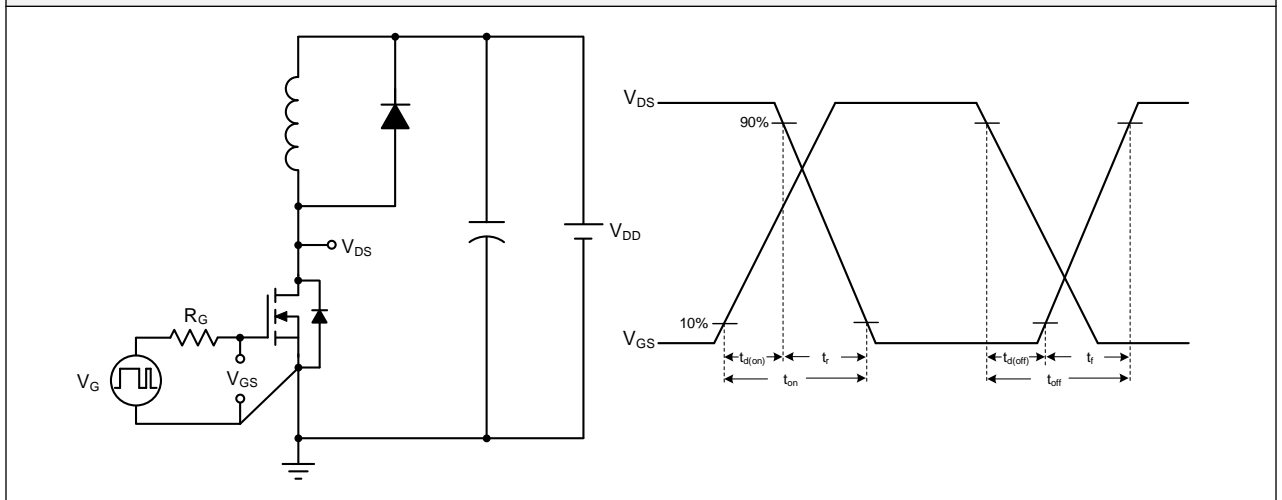
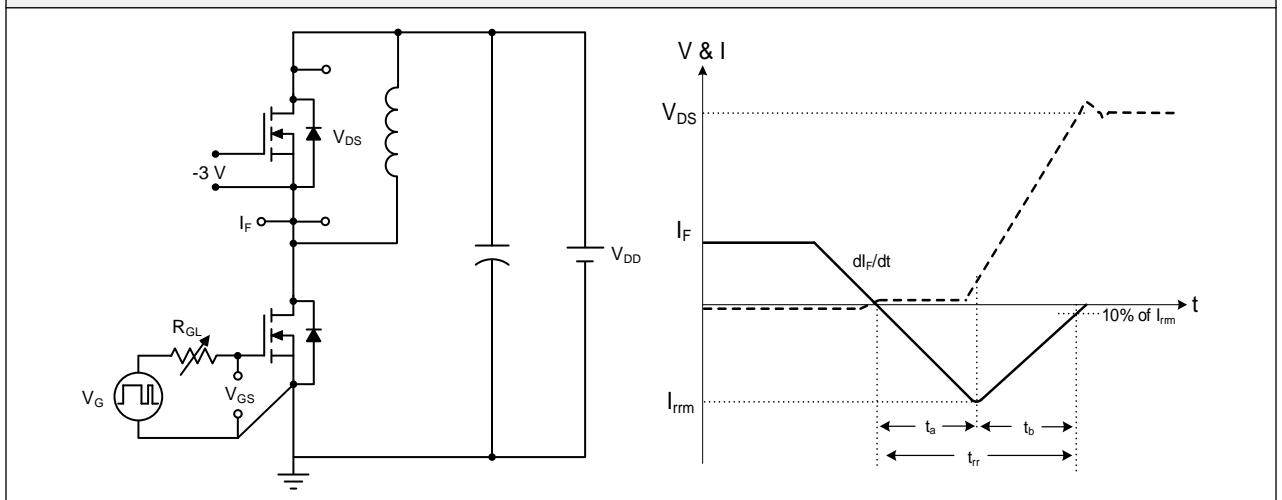
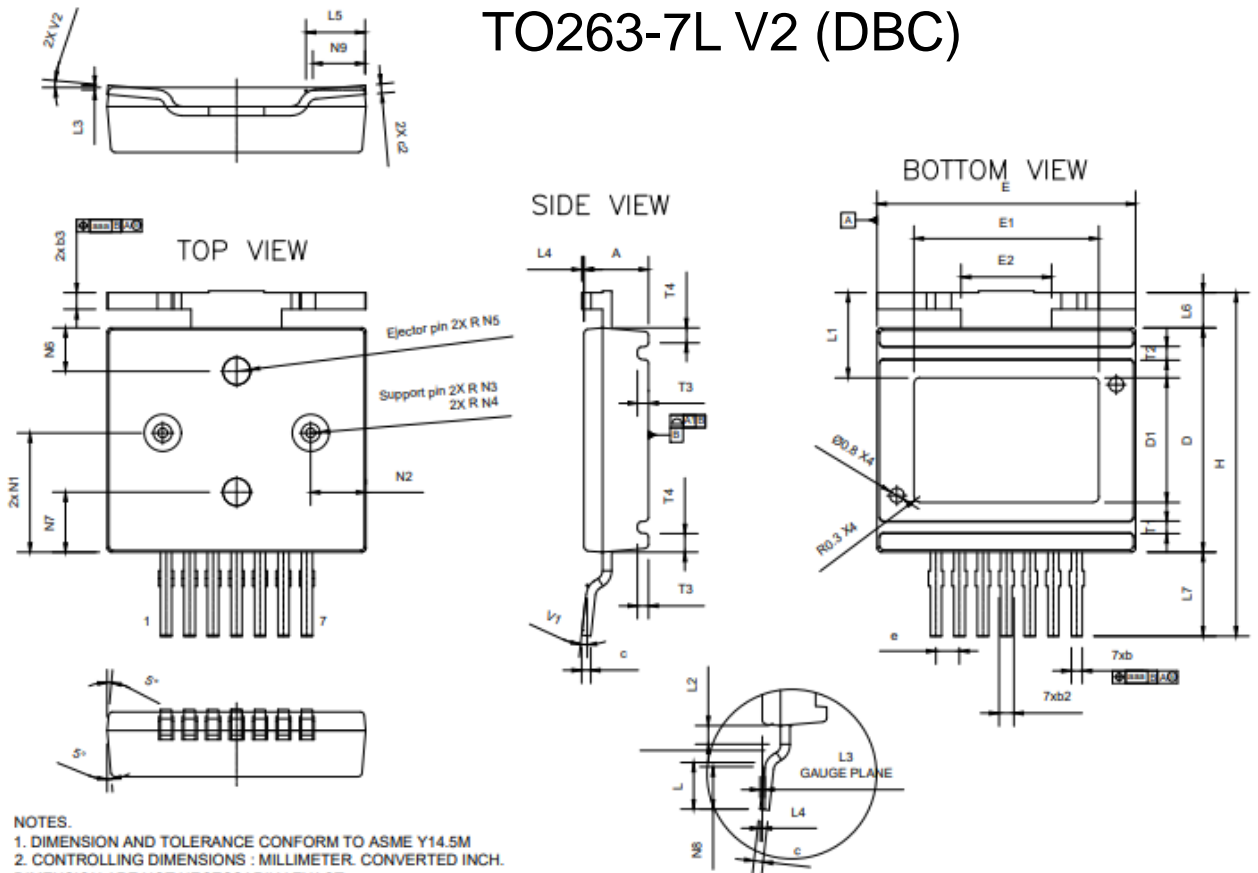


Figure 22. Peak Diode Recovery dv/dt Test Circuit and Waveforms



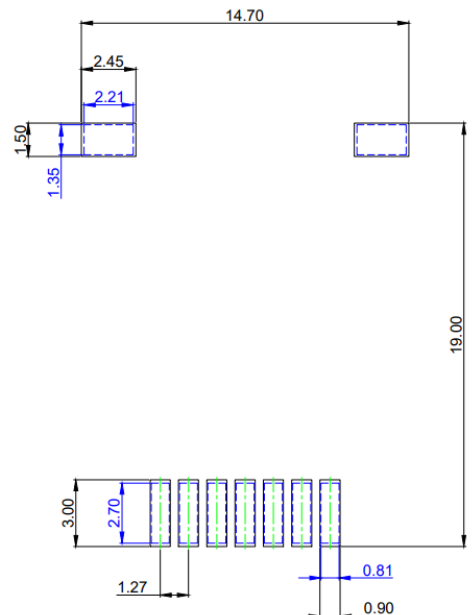
Package Outlines

TO263-7L V2 (DBC)



- NOTES.
1. DIMENSION AND TOLERANCE CONFORM TO ASME Y14.5M
 2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH. DIMENSION ARE NOT NECESSARILY EXACT.
 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 5. UNMARKED ROUND DIMENSIONS OF EMC ARE 0.2MM

[Footprint guide]



Package Outlines

SYMBOL	Common		
	DIMENSIONS MILLIMETER		
	MIN.	NOM.	MAX.
A	3.40	3.50	3.60
A1	0.05		
b	0.50	0.60	0.70
b2	0.70	0.80	0.90
b3	0.80	0.90	0.98
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	12.04	12.14	12.24
D1	6.29	6.74	7.34
E	13.90	14.00	14.10
E1	9.55	10.00	10.60
E2	4.85	4.90	4.95
e	1.27		
H	18.00	18.58	19.00
L	2.42	2.52	2.62
L1	4.60		
L2	0.90	1.00	1.10
L3	0.26		
L4	0.075	0.125	0.175
L5	3.09	3.19	3.29
L6	1.80	1.90	2.00
L7	4.44	4.54	4.64
N1	6.35	6.45	6.55
N2	2.95	3.00	3.05
N3	0.40	0.50	0.60
N4	0.20	0.25	0.30
N5	0.65	0.75	0.85
N6	2.25	2.35	2.45
N7	3.15	3.25	3.35
N8	2.185	2.285	2.385
N9	2.73	2.83	2.93
V1	0°	5°	8°
V2	0°	6°	8°
T1	0.69		
T2	0.74		
T3	0.60		
T4	1.00		
aaa	0.10		